



AON6712
N-Channel Enhancement Mode Field Effect Transistor
SRFET™



General Description

The AON6712 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. This device is suitable for use as a high side switch in SMPS and general purpose applications. *Standard Product AON6712 is Pb-free (meets ROHS & Sony 259 specifications).*

Features

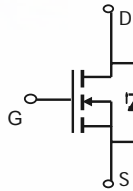
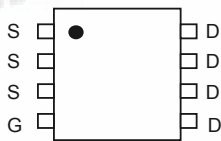
- V_{DS} (V) = 30V
- I_D = 20A (V_{GS} = 10V)
- $R_{DS(ON)} < 5.5m\Omega$ (V_{GS} = 10V)
- $R_{DS(ON)} < 6.5m\Omega$ (V_{GS} = 4.5V)

Fits SOIC8 footprint !



DFN5X6

Top View



SRFET™
 Soft Recovery MOSFET:
 Integrated Schottky Diode

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ^{B,J}	$T_C=25^\circ\text{C}$	30	A
	$T_C=100^\circ\text{C}$	30	
Pulsed Drain Current	I_{DM}	80	
Continuous Drain Current ^H	$T_A=25^\circ\text{C}$	16	A
	$T_A=70^\circ\text{C}$	13	
Avalanche Current ^C	I_{AR}	42	A
Repetitive avalanche energy $L=0.3\text{mH}$ ^C	E_{AR}	264	mJ
Power Dissipation ^B	$T_C=25^\circ\text{C}$	62.5	W
	$T_C=100^\circ\text{C}$	25	
Power Dissipation ^A	$T_A=25^\circ\text{C}$	2.5	W
	$T_A=70^\circ\text{C}$	1.6	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	14.2	20	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		Steady-State	42	50
Maximum Junction-to-Case ^C	$R_{\theta JC}$	1.2	2.0	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}$, $V_{GS}=0\text{V}$ $T_J=125^\circ\text{C}$			0.1 10	mA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 12\text{V}$			0.1	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.4	1.7	2.3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	80			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=20\text{A}$ $T_J=125^\circ\text{C}$		4.3	5.5	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=20\text{A}$		5.2	6.5	
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=20\text{A}$		100		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.35	0.5	V
I_S	Maximum Body-Diode Continuous Current				5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=15\text{V}$, $f=1\text{MHz}$		3940	5120	pF
C_{oss}	Output Capacitance			590		pF
C_{riss}	Reverse Transfer Capacitance			255		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		0.72	1.1	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $I_D=20\text{A}$		72.8	95	nC
$Q_g(4.5\text{V})$	Total Gate Charge			35.0		nC
Q_{gs}	Gate Source Charge			10.4		nC
Q_{gd}	Gate Drain Charge			12.4		nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $R_L=0.83\Omega$, $R_{GEN}=3\Omega$		9.8		ns
t_r	Turn-On Rise Time			8.4		ns
$t_{D(off)}$	Turn-Off Delay Time			45		ns
t_f	Turn-Off Fall Time			10		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}$, $dI/dt=300\text{A}/\mu\text{s}$		36	43	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$, $dI/dt=300\text{A}/\mu\text{s}$		32		nC

A: The value of $R_{\theta JA}$ is measured with the device in a still air environment with $T_A=25^\circ\text{C}$.

B: The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsink is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=150^\circ\text{C}$.

G: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $\bar{T}=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

H: Surface mounted on a 1 in 2 FR-4 board with 2oz. Copper.

J: Maximum current is limited by bonding wire.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

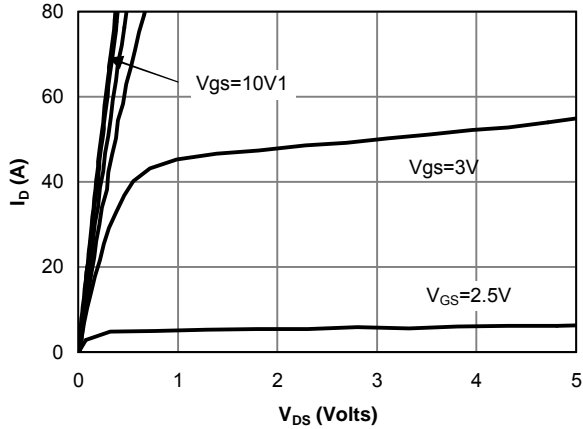


Figure 1: On-Region Characteristics

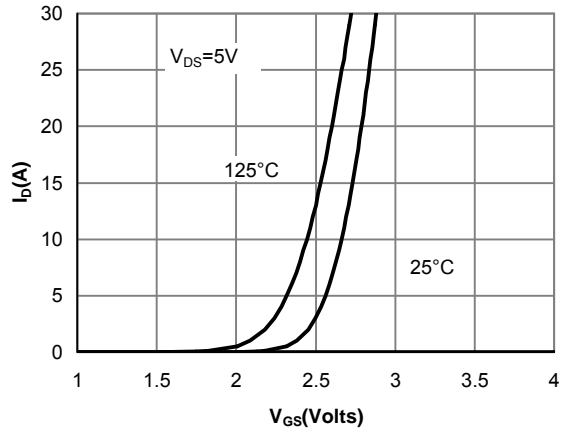


Figure 2: Transfer Characteristics

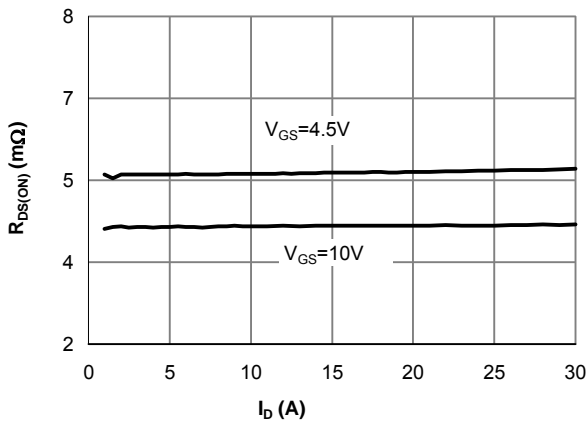


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

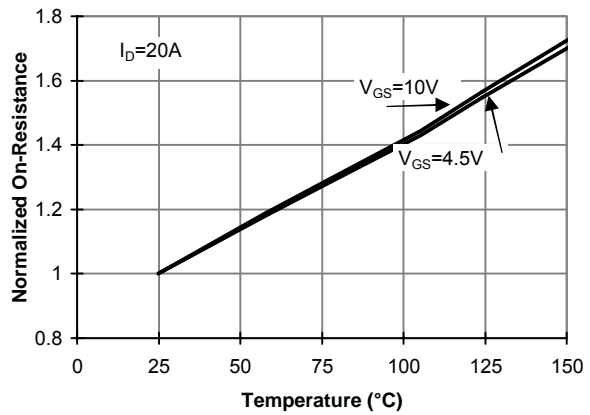


Figure 4: On-Resistance vs. Junction Temperature

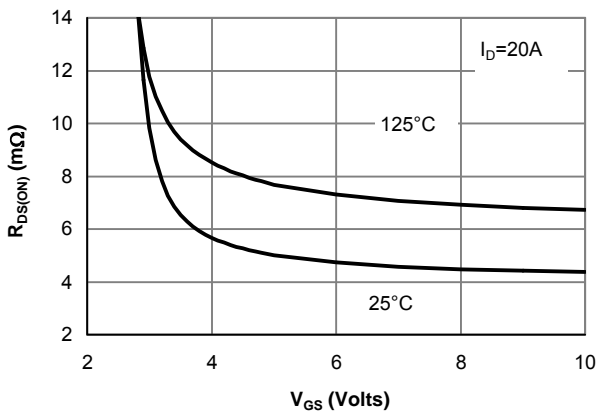


Figure 5: On-Resistance vs. Gate-Source Voltage

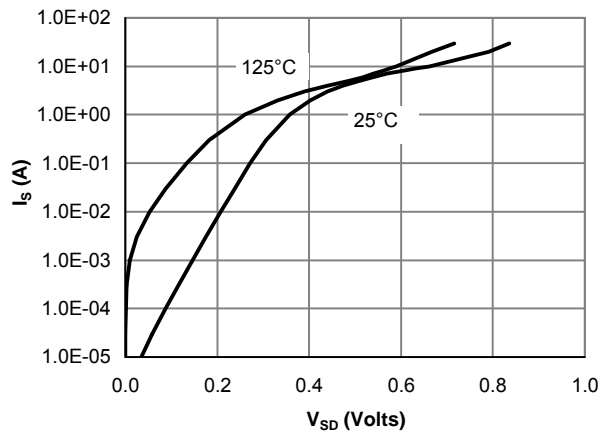


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

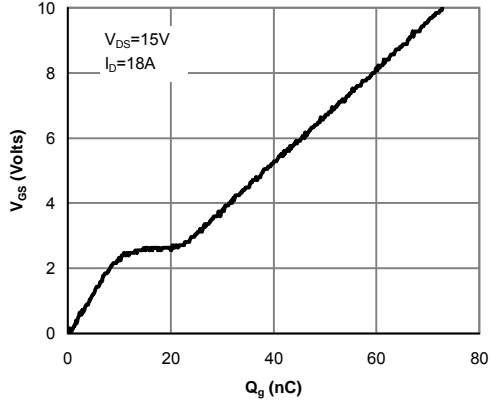


Figure 7: Gate-Charge Characteristics

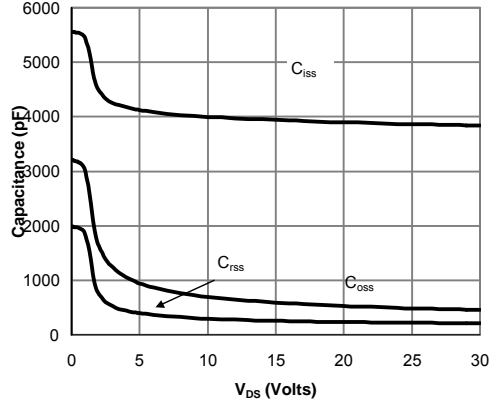


Figure 8: Capacitance Characteristics

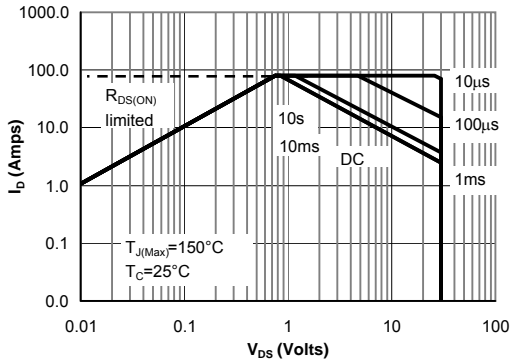


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

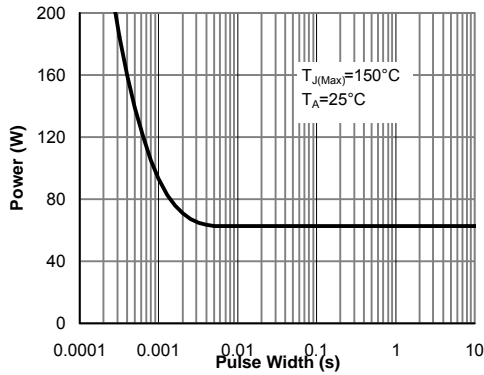


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

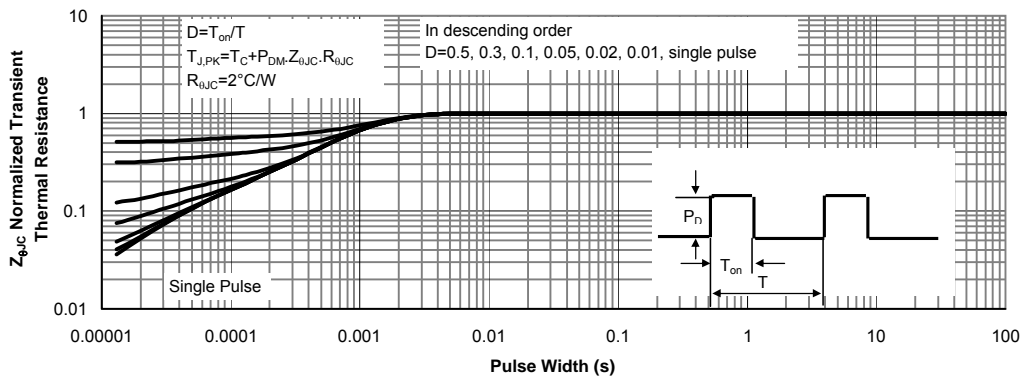


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

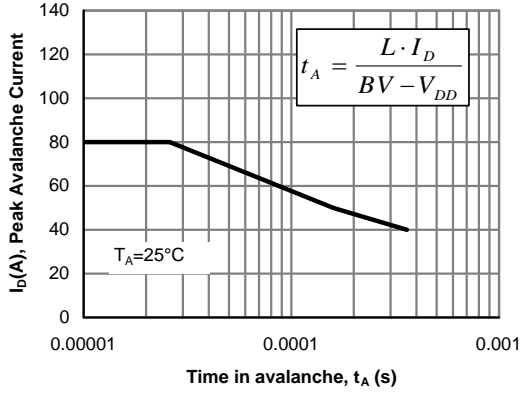


Figure 12: Single Pulse Avalanche capability

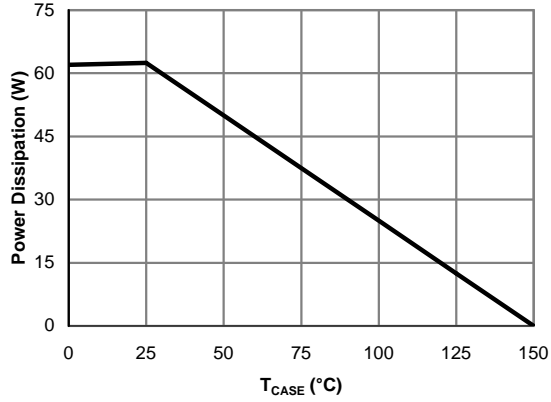


Figure 13: Power De-rating (Note B)

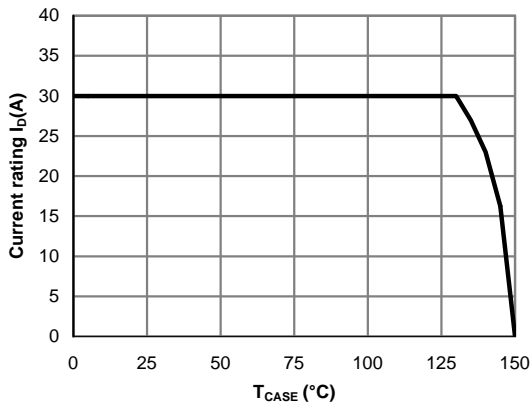


Figure 14: Current De-rating (Note B)

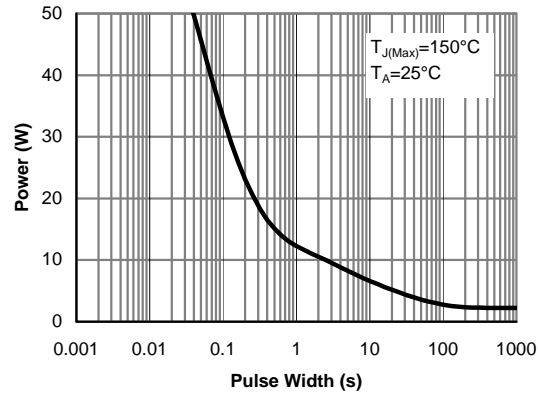


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note H)

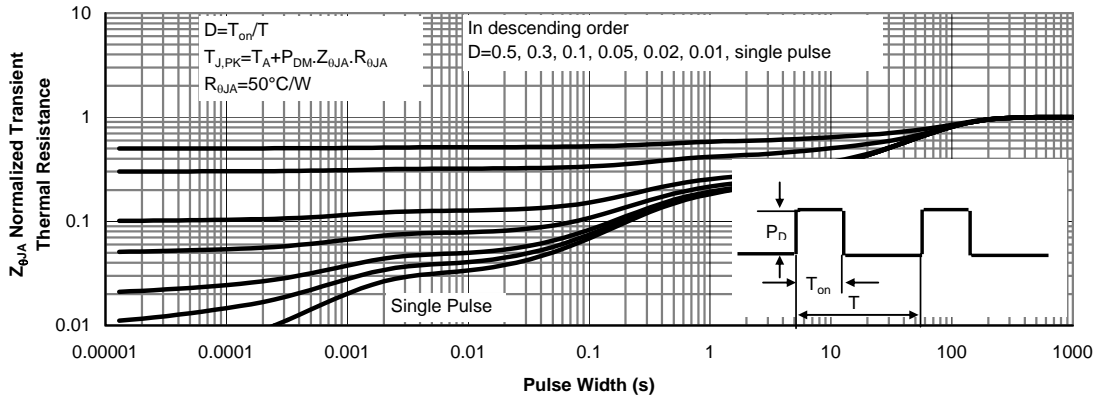


Figure 11: Normalized Maximum Transient Thermal Impedance (Note H)